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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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RITTER, LANG & KAPLAN
12930 SARATOGA AE. SUITE D1
SARATOGA, CA 95070

EXAMINER
TON, DAVID

ART UNIT	PAPER NUMBER
2133	22

DATE MAILED: 07/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/275,726	Devisoglu et al.
Examiner	**Group Art Unit**
D. Tom	2133

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication .
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

☑ Responsive to communication(s) filed on 4/14/03.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle,* 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☑ Claim(s) 1-22 is/are pending in the application.

Of the above claim(s)_____ is/are withdrawn from consideration.

☐ Claim(s)_____ is/are allowed.

☑ Claim(s) 1-22 is/are rejected.

☐ Claim(s)_____ is/are objected to.

☐ Claim(s)_____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The proposed drawing correction, filed on_____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on_____ is/are objected to by the Examiner.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 11 9(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number)_____.

☐ received in this national stage application from the International Bureau (PCT Rule 1 7.2(a)).

*Certified copies not received:_____.

Attachment(s)

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s)._____

☑ Notice of Reference(s) Cited, PTO-892

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Interview Summary, PTO-413

☐ Notice of Informal Patent Application, PTO-152

☐ Other_____

Office Action Summary

DETAILED ACTION

1. In view of the Appeal Brief filed on 4/14/03, PROSECUTION IS HEREBY REOPEN. New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

2. Claims 1-22 are presented for examination.

3. Applicant's arguments with respect to claims 1-22 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

4. Claim 19 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 19:

Claim 19, line 3, "said data capture unit" and "said system operation unit" lacks positive antecedent basis.

Claim Rejections - 35 USC § 103

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claims 1-8, 10-18, 20-22 are rejected under 35 U.S.C. § 103(a) as being unpatentable over **Veenstra et al. (Veenstra)** patent no. **6,460,148** in view of **Nelson** patent no. **5,369,684**.

As per claim 1:

Veenstra teaches the invention substantially as claimed, including an integrated circuit [PLD 16 of Fig. 6], having logic blocks [programmable logic device, col. 7 lines 19-34] comprising:

a control unit [control logic 274 of Fig. 6] for performing test and debug operations of said logic blocks of said integrated circuit [col. 18 lines 16-30];

a memory [sample memory 324 of Fig 8] associated with said control unit, said memory holding instructions for said control unit [col. 13 lines 10-20]; and

a plurality of probe lines [specified signal lines, col. 6 lines 19-27] responsive to said control unit for carrying system operation signals from predetermined probe points of said logic blocks, wherein said probe lines comprise strings of storage elements [capture register 620 and update register 630 of Fig. 13, col. 24 line 64 - col. 25 line 22] providing signal paths from said probe points to said memory, said signal paths capable of moving sets of said system operation signals at system

operation clock rates [PLD 16 may be operated real world environment and logic analyzer 260 may capture real test data, col. 24 lines 35-53], said sets of system operation signals stored in said memory so that said sets of operation signals are retrievable [see claim 1].

Veenstra does not explicitly teach integrating the PLD 16 of Fig. 5 including the JTAG port 272, the control logic 274 and embedded logic analyzer 260 into an integrated circuit. However, Veenstra teaches that "upon successful debugging of the PLD design, the PLD chip can be reprogrammed without the logic analyzer circuit, or the circuit can be left on the chip" [col. 5 lines 50-65].

Nelson teaches integrating the IC 10 [see Fig. 1] including a JTAG control 22 and a built-in self-test circuit (BIST 26 and 28) into an integrated circuit 10 [col.3 lines 4-16].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to integrate the PLD 16 as taught by Veenstra into an integrated circuit as taught by Nelson.. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so as a matter of design choice [see Veenstra, col. 5 lines 50-65] to provide a build-in self-test for the PLD.

As per claim 2:

Veenstra teaches a plurality of scan lines responsive to said control unit for loading test signals for said logic blocks [Fig. 15] and retrieving test signal results from said logic blocks [Fig. 16], said test signals and said test signal results stored in said memory so that said loading and retrieving operations are performed to said integrated circuit [col. 26 lines 11-32].

As per claim 3:

Veenstra teaches the integrated circuit further comprising a unit [JTAG port 272 of Fig. 6] coupled to said control unit and said memory, said unit testing said logic blocks and said memory responsive to and in cooperation with said control unit to self-test said integrated circuit.

As per claim 4:

Veenstra teaches the scan lines comprise a first string of flip-flop connectors [test register 804 of Fig. 14] connected between a logic block and the remainder of said integrated circuit proximate said logic block, said flip-flop connectors providing signal paths between said logic block and the remainder of said integrated circuit proximate said logic block in one mode and carrying test signals and test signal results in a second mode [see Fig. 13, col. 24 line 64 - col. 25 line 22].

As per claim 5:

Veenstra teaches the scan lines comprise a second string of flip-flop connectors [test register 808 of Fig. 14] between elements of a logic block, said flip-flop connectors providing signal paths between said logic block elements in one mode and carrying test signals and test signal results in a second mode [see Fig. 13, col. 24 line 64 - col. 25 line 22].

As per claim 6:

Veenstra teaches each of said probe lines comprises a string of programmable connectors providing a signal path for carrying system operation signals at predetermined probe points of said logic blocks in one mode [see Fig. 13].

As per claim 7:

Veenstra teaches each programmable connector of said probe lines is programmed by flip-flop connector, each flip-flop connector connected between elements of said integrated circuit and forming

part of string of flip-flop connectors, said flip-flop connectors providing signal path between said integrated circuit elements in one mode and carrying signal for programming said programmable connectors in a second mode [see Fig. 13].

As per claim 8:

Veenstra teaches at least some of said probe lines comprises a string of programmable connector providing a signal path for carrying digital state system operation signals [see Fig. 13].

As per claim 10:

Veenstra teaches the invention substantially as claimed, including an integrated circuit [PLD 16 of Fig. 6] comprising:

an interface [JTAG Port 272 of Fig. 6] for coupling to an external diagnostic processor;

a unit [embedded logic analyzer 260 of Fig. 6] responsive to instructions from said external diagnostic processor for capturing sets of sequential system operation signals of said integrated circuit;

a plurality of lines [Data in [15:0] of Fig. 8] coupled to said unit for carrying said system operation signals from predetermined points of said integrated circuit to said memory, wherein said lines providing signal paths from said point to said memory, said signal path capable of moving sets of said system operation signals at system operation clock rates [PLD 16 may be operated real world environment and logic analyzer 260 may capture real test data, col. 24 lines 35-53], said sets of system operation signal stored in said memory so that said sets of system operation signal are retrievable [see claim 1].

a memory [RAM 324 of Fig. 8] coupled to said unit and to said interface, said sets of sequential system operation signals stored in said memory at one or more clock signal rates internal to said integrated circuit [PLD may be operated in a real-word environment, col. 24 lines 35-53] and retrieved from said memory through said interface to said external process at one or more clock signal rates external to said integrated circuit [TCLK of Fig. 6] so that said external diagnostic processor [computer system 18 of Fig. 5] can process said capture system operation signals [see claim 1].

Veenstra does not explicitly teach integrating the PLD 16 of Fig. 5 including the JTAG port 272, the control logic 274 and embedded logic analyzer 260 into an integrated circuit. However, Veenstra teaches that "upon successful debugging of the PLD design, the PLD chip can be reprogrammed without the logic analyzer circuit, or the circuit can be left on the chip" [col. 5 lines 50-65].

Nelson teaches integrating the IC 10 [see Fig. 1] including a JTAG control 22 and a built-in self-test circuit (BIST 26 and 28) into an integrated circuit 10 [col.3 lines 4-16].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to integrate the PLD 16 as taught by Veenstra into an integrated circuit as taught by Nelson.. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so as a matter of design choice [see Veenstra, col. 5 lines 50-65] to provide a build-in self-test for the PLD.

<u>As per claims 11-12:</u>

Veenstra teaches said unit further comprises trigger logic responsive to said system operation signals for initiating storage of a set of said system operation signals in said memory [col.13 lines 10-19 and lines 35-40].

As per claim 13:

Veenstra teaches each of said probe lines comprises a string of programmable connector [see Fig. 13] providing a signal path for carrying system operation signals at predetermined probe points in one mode [col. 24 line 54 - col. 25 lines 22].

As per claim 14:

Veenstra teaches each programmable connector of said probe lines is programmed by a flip-flop connector connected between elements of said integrated circuit and forming part of string of flip-flop connectors [Fig. 13], said flip-flop connectors providing signal paths between said integrated circuit elements in one mode and carrying signal for programming said programmable connectors in a second mode [col. 24 line 54 - col. 25 lines 22].

As per claim 15:

Veenstra teaches the invention substantially as claimed, including a method of operating an integrated circuit [PLD 16 of Fig. 6] having logic blocks, a control unit, a memory and a plurality of lines of said logic blocks [see claim 10 above], said method comprising:

operating said logic blocks to perform normal system operations [PLD 16 may be operated real world environment and logic analyzer 260 may capture real test data, col. 24 lines 35-53] at one or more system clock signal rates [col. 13 lines 31-38] internal to said integrated circuit to produce sets of system operation signals [complex pattern of signals, see col. 13 lines 39-56];

enabling [inherently in claim 4] said lines responsive to said control unit to capture and carry said sets of system operation signals of said logic blocks at said system clock signal rates internal to said integrated circuit;

retrieving [inherently in claim 4] said sets of system operation signals from said logic blocks along said lines at said system clock signal rates internal to said integrated circuit;

storing [claim 4] said sets of system operation signals in said memory at said system clock signal rates internal to said integrated circuit; and

processing [inherently in claim 4] said sets of stored system operation signals to perform test and debug operations of said logic blocks of said integrated circuit.

Veenstra does not explicitly teach integrating the PLD 16 of Fig. 5 including the JTAG port 272, the control logic 274 and embedded logic analyzer 260 into an integrated circuit. However, Veenstra teaches that "upon successful debugging of the PLD design, the PLD chip can be reprogrammed without the logic analyzer circuit, or the circuit can be left on the chip" [col. 5 lines 50-65].

Nelson teaches integrating the IC 10 [see Fig. 1] including a JTAG control 22 and a built-in self-test circuit (BIST 26 and 28) into an integrated circuit 10 [col.3 lines 4-16].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to integrate the PLD 16 as taught by Veenstra into an integrated circuit as taught by Nelson.. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so as a matter of design choice [see Veenstra, col. 5 lines 50-65] to provide a build-in self-test for the PLD.

As per claims 16-17:

Veenstra teaches said system operation signals comprise sequential system operation signal [col. 13 lines 39-56].

As per claim 18:

Veenstra teaches the invention as claimed, including an integrated circuit has a plurality of scan lines of said logic blocks comprising:

loading said memory with test signals and instructions for said control unit;

loading said scan lines responsive to said control unit with said test signals for said logic blocks at one or more clock signal rates internal to said integrated circuit;

operating said logic blocks at one or more system clock signal rates [col. 13 lines 31-38] internal to said integrated circuit;

retrieving [inherently in claim 4] said sets of system operation signals from said logic blocks along said lines at said system clock signal rates internal to said integrated circuit;

storing [claim 4] test signal result from said logic blocks along said scan lines at one or more clock signal rates internal to said integrated circuit; and

processing [inherently in claim 4] said stored test results signals in said control unit responsive to said stored instructions in said memory to perform test and debug operations of said logic blocks of said integrated circuit.

As per claims 20-21:

Veenstra teaches said system operation signals comprise sequential system operation signals [col. 13 lines 39-56].

As per claim 22:

Veenstra teaches said system operation signals are stored in said memory at one or more clock signal rates internal to said integrated circuit [col. 13 lines 31-18].

7. Claims 9 is rejected under 35 U.S.C. § 103(a) as being unpatentable over **Veenstra et al. (Veenstra)** patent no. **6,460,148** in view of **Nelson** patent no. **5,369,684** and further in view of **Fisch** patent no. **5,254,482**.

As per claim 9:

Veenstra and Nelson do not teach signal path for carrying signal reflective of analog conditions.

Fisch teaches a ferroelectric capacitor test structure for chip die. The test structure connect to bond pads of the die so that analog tests can be conducted thereon under various analog conditions to determine aging, fatigue, etc. [col. 10 lines 20-47].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the netlist of Veenstra to include a signal path for carrying signal reflective of analog conditions as taught by Fisch. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so as a matter of design choice [see Veenstra, col. 15 lines 35-47, Fig. 4] to provide a build-in self-test for the PLD as taught by Nelson.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Ton, whose telephone number is (703) 306-3043. The examiner can normally be reached Monday through Thursday from 6:30 AM to 4:00 PM and alternate Friday from 6:30 AM to 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady, can be reached at (703) 305-9595.

Any inquiry of a general nature of relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to: (703) 746-7239 (Official)

(703) 746-7240 (Non-Official)

(703) 746-7238 (After-Final)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

dt

June 03, 2003

DAVID TON
PRIMARY EXAMINER